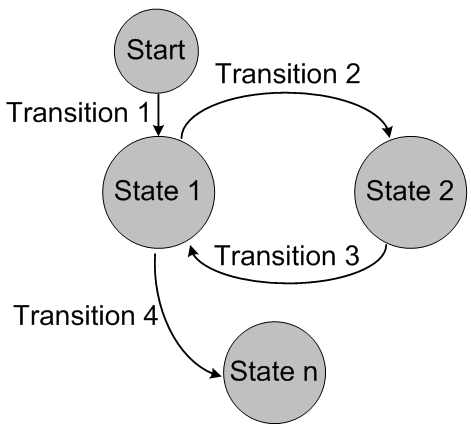
(College logo)



**Project synopsis on**

**DESIGN OF STATE MACHINE USING XILINX/VHDL**

Under taken by:

Name 1 Roll no. 1 Name 2 Roll no. 2

Name 3 Roll no. 3 Name 4 Roll no. 4

**ABSTRACT:**

Xilinx is a technology company which is provides programmable logic devices and known for inventing FPGA. FPGA (Field Programmable Gate Array) are semiconductor device which are based on configurable logic blocks connected via various interconnects according to the required feature. Xilinx is used to for synthesis and analysis of HDL designs, enabling the developer to synthesize ("compile") their designs, perform timing analysis, examine RTL diagrams, simulate a design's reaction to different stimuli, and configure the target device. Using Xilinx we can design Finite State Machine and perform various analyses. The analysis will be based on the designing of state machine using state diagram and state table.

**ABOUT THE TECHNOLOGY:**

State machines are nothing but a device that can be stable in more than one set of states. Its output depends on present input and present state. It can be distinguished into two groups-

**Mealy and Moore Circuits-** In the theory of computation, a Mealy machine is a finite-state machine whose output values are determined both by its current state and the current inputs.

This is in contrast to a Moore machine, whose output values are determined solely by its current state.

**WORKING PRINCIPLE:**

In Xilinx, the analysis is done in the following steps-  
1. **Synthesis** – The execution of coding logic which need to be implemented.

2. **View RTL Schematic**- It shows a representation of the pre-optimized design in terms of generic symbols, such as adders, multipliers, counters, AND gates, and OR gates, that are independent of the targeted Xilinx device.

3. **Test Bench** – It’s used to stimulate the values depending upon the input and state provided.

**SOFTWARE USED**

1. Xilinx ISE 9.2

**APPLICATIONS:**

**1. Performance Analysis:** Xilinx stimulation can be used to analyze performance of the programmable logic device based. Complexity can be significantly reduced using the analysis.

**2.** **Functional testing**: It helps in testing of the FPGA or PLD based on the stimulation process and equating it’s performance with the real world application.

**3. Designing:** It’s used to design Field Programmable Gate Array (FPGA) which on instance used for configuring logic blocks with conditional interconnects.

**REFERENCES:**

* <http://noel.feld.cvut.cz/hw/amd/90005a.pdf>
* <https://www.xilinx.com/support/documentation/sw_manuals/help/iseguide/mergedProjects/destech/html/cd_fsm.html>
* <https://www.xilinx.com/support/documentation/university/ISE-Teaching/HDL-Design/14x/Nexys3/Verilog/docs-pdf/lab10.pdf>

**BASICS OF XILINX:**

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**SAMPLE XILINX PROGRAM:**

Implementation of AND GATE using Behavioral Model:

